Yield Considerations for Ion-Implanted GaAs MMIC's

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Abstract—**An ion-implantation based process is described for fabricating GaAs monolithic microwave integrated circuits (MMIC's) incorporating active devices, RF circuitry, and bypass capacitors. Low ohmic contact resistance and good control of metal–insulator–metal (MIM) capacitance values is demonstrated and some factors affecting FET and capacitor yield are discussed. High dc yield of typical amplifier circuits is shown indicating that this process has the potential for achieving very high overall yields in a production environment. Good yield of functional MMIC modules with multicircuit complexity is projected.**

I. Introduction

AN ION-IMPLANTATION based process has been developed for the fabrication of gallium arsenide monolithic microwave integrated circuits (MMIC's) incorporating active devices, RF circuitry, and all bypass capacitors. Multiple, localized ion implantation in semi-insulating GaAs substrates [1] is used for forming optimized active layers and n^+ contacts for low noise and power FET's, mixer diodes, etc. In addition to providing a planar structure, this approach allows the flexibility of accommodating different active layers on the same substrate as required for optimizing the performance of different devices in the circuit. Contact photolithography is used for all pattern steps. Silicon nitride deposited by plasma enhanced CVD is used as the dielectric in metal–insulator–metal (MIM) capacitors and as the insulator in a two level metallization process. Excellent uniformity and reproducibility of MIM capacitors has allowed their use for both RF tuning and bypassing. Except resistors, all microwave circuitry, air bridges, and beam leads are on the second metallization level which is electroplated to a thickness of 2–3 μm to minimize losses. Backside through-substrate via holes are etched where necessary. This paper presents an overview of the fabrication process and discusses yield limiting factors which have been investigated. The data presented here have been obtained on a process diagnostic test pattern [2] (Fig. 1) present on all our MMIC mask sets.

II. Fabrication Process

Fig. 2 is a schematic drawing of the various active and passive components comprising an MMIC. These include low noise and power MESFET's, Schottky-barrier diodes, thin film and bulk resistors, MIM capacitors for RF tuning and bypassing, transmission lines, air bridges, and backside through-substrate via holes. A pictorial representation of the fabrication procedure is given in Fig. 3. As shown there, fabrication of an MMIC begins with the synthesis of doping profiles for FET active layers, n^+ contacts and bulk resistors by localized Si^+ ion implantation in qualified semi-insulating GaAs substrates. Photoresist is used as the implantation mask. Substrate qualification consists of sampling the front and the tail of the ingot under consideration and checking the doping profile for a standard implant-cap-anneal cycle. Activation, pinch off voltage uniformity, and electron mobility are measured and compared with design specifications to determine the suitability of the ingot for the MMIC process. The isolation afforded by the SI substrate after undergoing an annealing cycle is also checked. A sheet resistance $\geq 10^7\ \Omega/\square$ is required for passing this test. Fig. 4 shows the reproducibility of a 100-keV Si-implantation profile in different types of substrates, processed at different times. The minor profile variations observed arise as a result of differences in substrate background doping and compensation and may be corrected by slight adjustment of implant schedules based on qualification data. Additional data for a different im-

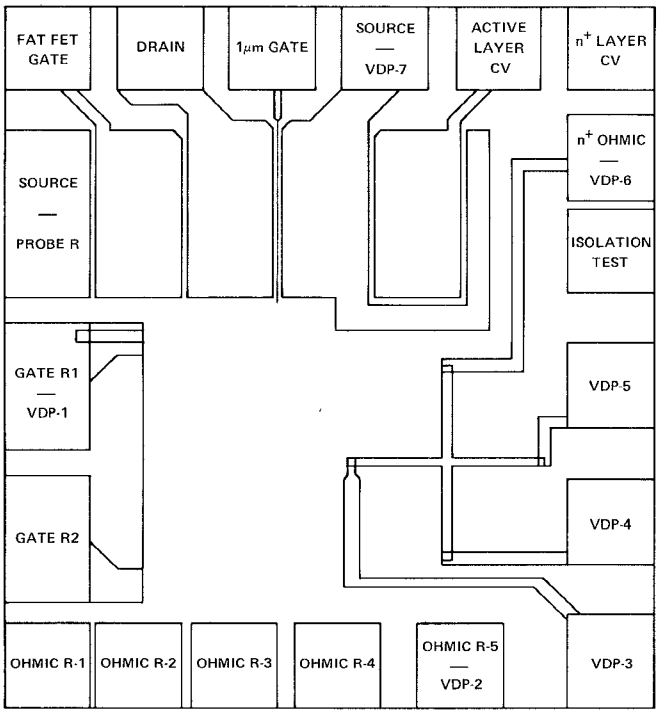

Fig. 1 Schematic diagram showing the process monitor test pattern.

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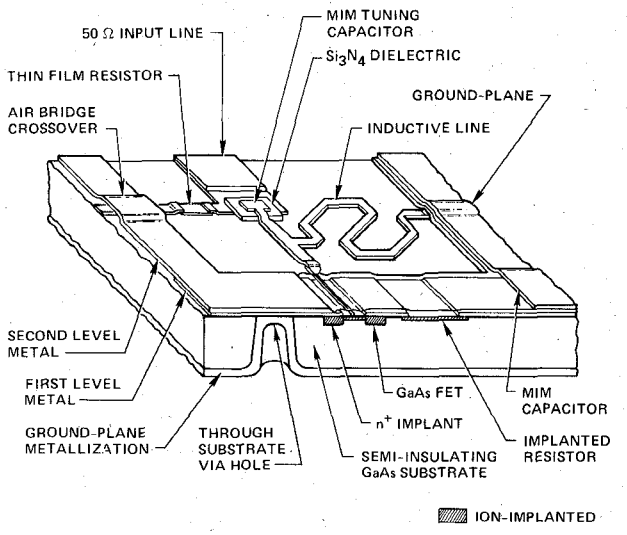


Fig. 2. Schematic drawing of an MMIC showing typical components needed.

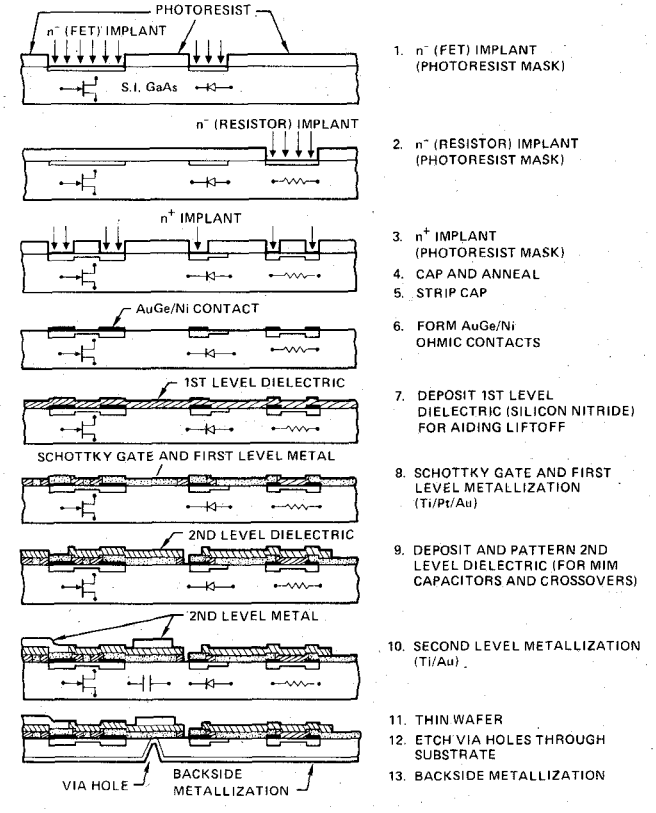


Fig. 3. Pictorial representation of MMIC fabrication process.

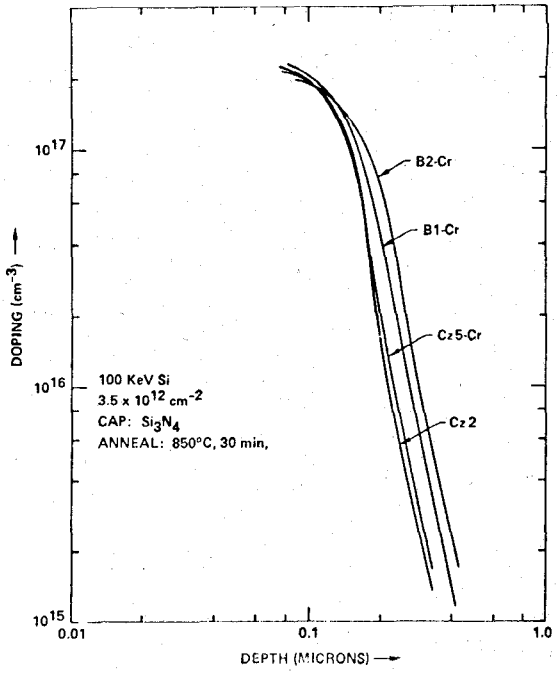


Fig. 4. Doping profiles in LEC and Bridgman semi-insulating GaAs substrates.

TABLE I
ACTIVE LAYER UNIFORMITY
(Implant: 5E12 cm^{-2}, 225 keV Si; 5E12 cm^{-2}, 40 keV Si)

ID	Substrate Type	$\langle I_{dss} \rangle$ mA Before Gate Recess	σ (%)
A	Undoped LEC	217.5	2.3
B	Undoped LEC	217.4	2.3
C	Undoped LEC	195.5	0.92
D	Cr-doped Bridgman	193.4	2.0
E	Cr-doped Bridgman	196.8	2.3
F	Cr-doped Bridgman	201.0	4.4

$\langle I_{dss} \rangle$ = 203.6 mA
σ_{IDSS} = 11.0 mA (5.4%)

plant schedule are provided in Table I where the average I_{dss} before gate recess of 200-μm wide FET's is given for various substrates. These wafers were also processed separately and the data show excellent uniformity and reproducibility of active layers made possible by direct ion implantation in SI GaAs.

Following active layer formation, ohmic contacts are defined by sequential evaporation of Au–Ge and Ni, liftoff, and alloying at 450°C. This metallization scheme results in low resistance contacts quite reliably as evidenced by the data in Table II. These data were obtained on randomly selected wafers at the completion of front-side processing and show that it is possible to maintain a low specific contact resistance ($\sim 1 \times 10^{-6}$ Ω·cm^2) through the 250°C silicon nitride deposition steps. The observed variation of specific contact resistance shown in Table II represents a combination of measurement error and actual resistance variation but contributes less than 10-percent variation to FET source resistance.

After contact metallization, the 1.0-μm gates are defined by contact photolithography, recess etch, Ti–Pt–Au evaporation, and liftoff. At present, gate yield is a significant circuit yield limiting factor. Some preliminary data are given in Table III where yields have been averaged over several wafers processed. The criterion "other process related defects" includes damage due to wafer handling, poor

TABLE II
SPECIFIC CONTACT RESISTANCE RESULTS
(After Completion of all MMIC Process Steps)

Metallization : AuGe/Ni		
Date Measured	ID	$\langle R_c \rangle$ (10^{-6} Ω cm^2)
10/80	SP-100	0.51
	SP-101	0.66
	SP-102	1.31
	R2C-IL5	0.51
	15-2	0.99
	16-1	0.49
	W7-1	1.6
	W7-2	1.7
Through	G19H-111	3.3
	W9-1	0.91
	W12-2	2.5
	W19-1	0.86
	60-1	3.1
	42-2	2.5
	40-1	0.56
	531	0.84
	71S421	0.30
	41-2	0.86
5/82	511	1.1

$\langle R_c \rangle = 1.3 \times 10^{-6}$ Ω cm^2
$\sigma = 0.92 \times 10^{-6}$ Ω cm^2

TABLE III
FET DC YIELD
($\langle I_{dss} \rangle = 47.1$ mA; $\sigma = 5.5$ mA (11.6%))

Criterion	FET Yield for Different Gate Widths, Gate Length = 1.0 μm		
	Width = 200 μm, S-D gap = 3.8 μm	Width = 500 μm, S-D gap = 4.8 μm	Width = 990 μm, S-D gap = 4.8 μm
Broken Gate	0.90	0.94	0.82
Other Process Related Defects	0.92	0.98	0.95
Net Yield	0.83	0.92	0.78

source–drain definition, and shorts caused by metallization defects normally found with contact photolithography. The lower yield of 200-μm wide FET's as compared to the 500-μm wide FET's is probably due to the smaller source–drain gap of the 200-μm wide device. These data were obtained on ~10 cm^2 (half of a 2-in wafer) GaAs wafers. In order to maximize gate yield several precautions have to be taken. These include monitoring wafer flatness and ensuring that it is in the range of ±1 μm/in after capping and annealing, and using 0.090-in thick lithographic masks for minimum runout from mask bowing during contact printing.

Gate metal definition is followed by Ti/Au first level metallization which provides overlays for ohmic contacts and the lower electrodes of MIM capacitors. This first level metal pattern is defined by ion milling through a photoresist mask to remove unwanted areas so as to achieve rounded edges of the remaining metal which are necessary for good capacitor yield as discussed below. A 6000-Å layer of silicon nitride is deposited next using plasma enhanced chemical vapor deposition (PSN). This forms the dielectric for MIM capacitors and the crossover insulator in a two level metallization scheme. Finally, the second metal layer is defined by photolithography and gold electroplating to a thickness of 2 to 3 μm. It provides the top

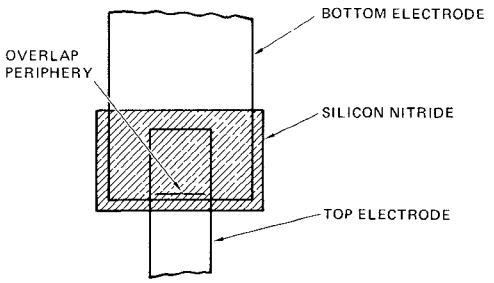


Fig. 5. Schematic diagram of a metal–insulator–metal (MIM) capacitor.

TABLE IV
METAL–INSULATOR–METAL CAPACITORS
(Insulator: 6000-Å Silicon Nitride Deposited by Plasma Enhanced CVD)

Approx. Measurement Date	ID Number	Average Cap. pF/mm^2	σ (%)	
6/80	143	125	2.1	
	165	132	2.1	
	173	132	3.4	measured on in-
	174	128	1.9	process wafers
	175	131	2.4	
	R5M/18	125	1.8	
	1265	135	3.2	
Through	1357-1	127	<0.3	
	1357-2	133	<0.3	
	1393	125	<0.3	
	1398	125	<0.3	measured on test
	1412	125	<0.3	chips
	1424	136	<0.3	
	1432	138	<0.3	
2/82	1439	139	<0.3	

Mean = 130 pF/mm^2
σ = 3.9%
N = 15

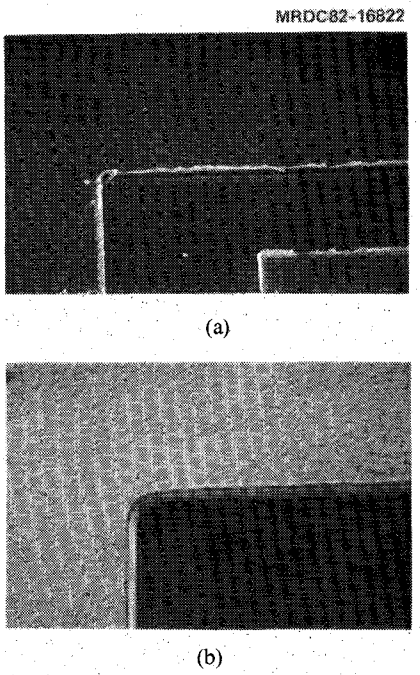
electrode of MIM capacitors, all interconnects, air bridges, and other microwave circuitry.

The uniformity, reproducibility, and dc yield of MIM capacitors have been studied. Data on the first two aspects is given in Table IV. These data, obtained on randomly selected wafers, span a period of 20 months and clearly indicate that by adequately monitoring the deposition process it is possible to have a tight control on the thickness and dielectric constant of the PSN. Such control has encouraged the use of MIM capacitors for RF tuning as well as bypassing. The first group of data in Table IV were obtained on actual wafers in process and the σ value reflects variations in both the PSN and the electroplated top electrode of the small (100 μm × 100 μm) test capacitors. Remaining data were obtained on test wafers where the top electrode was formed by liftoff. Negligible variation in capacitance values was observed in these cases.

DC yield of MIM capacitors was found to depend on both the area and the length of overlap periphery (Fig. 5) between the first and the second metallization levels. It was possible to get a good fit of measured yield data using multiple linear regression techniques to a linearized equation (valid for yields near unity) of the form

$$Y = 1 - \alpha A - \beta P$$

as shown in Table V where all the terms have also been defined. The last column of Table V shows the contribution to circuit yield of 5 typical (10 pF) bypass capacitors and clearly indicates the importance of this problem. The



(a)

(b)

Fig. 6. (a) Sharp pattern edges obtained by direct liftoff of Ti(500 Å)/Au(4000 Å). (b) Smooth edges obtained by ion milling the metallization pattern.

TABLE V
DC YIELD OF MIM CAPACITORS
(Insulator: 6000-Å Silicon Nitride Deposited by Plasma Enhanced CVD)

$Y = 1 - \alpha A - \beta P$
Y = DC Yield
A = Capacitor Area (mm^2)
P = Overlap Periphery Between First and Second Metallization Levels (mm)

ID Number	α mm^{-2}	β mm^{-1}	RMS Prediction Error $\sqrt{\frac{\sum}{i}(y-y_i)^2}$	Yield of 10 pF Bypass Cap with Dimensions of A = 0.077 mm^2 P = 0.5 mm	Contribution to Circuit Yield Assuming 5 Bypass Capacitors
E	0.83	0.15	0.080	0.86	0.47
F	0.16	0.20	0.046	0.89	0.56
G	0.66	0.013	0.016	0.94	0.73

area dependence of capacitor yield is due to a pinhole density in the PSN. In practice, pinholes in the nitride are associated with debris on the wafer, metal splattering during first level metallization, etc., and can be reduced by controlling these factors. The overlap periphery dependence arises due to the sharp edges (as obtained by direct liftoff, Fig. 6(a)) which are not well covered by PSN and usually result in a short. Rounded edges as obtained by ion milling or special liftoff techniques [3] (Fig. 6(b)) are more reliably covered by PSN and cause fewer shorts. The improvement in capacitor yield attributable to improved processing of the first level metal may be seen from the dramatic reduction of β for wafer *G* which had ion milled first level metal compared to wafers *E* and *F* which were processed earlier and had first level metal defined by direct liftoff. The periphery problem can be effectively circumvented by using an airbridge to contact the top capacitor electrode but this approach may result in added process complexity (unless airbridges are being used elsewhere in the circuit) and constraints on circuit layout.

TABLE VI
DC CIRCUIT YIELD

	Buffer Amplifier	Driver Amplifier	Power Amplifier
Total Gate Periphery (mm)	0.2	1.0	1.98
Source-Drain Gap (μm)	3.8	4.8	4.8
Total MIM Capacitance (pF)	20	49.4	50.8
FET Yield (%)	81	86	59
Capacitor Yield (%)	97	88	76
Circuit Yield (%)	78	76	47

Preliminary data on dc probe plus visual (microscopic inspection) circuit yield of three different circuits are presented in Table VI. These data were obtained at the completion of front side processing and do not include attrition due to subsequent steps involving thinning, via hole etching, backside metallization and sawing. The data depicted in Table VI are commensurate with FET and capacitor yields presented earlier (with improved processing) and represent some of the highest yields observed using the above described MMIC fabrication process. These data indicate the potential for achieving high overall yields of functional MMIC modules with multicircuit complexity. For example, a module consisting of the three circuits described in Table VI would have an overall dc yield of about 28 percent before backside processing.

III. CONCLUSIONS

An ion-implantation based process has been developed for fabricating GaAs MMIC's incorporating active devices, RF circuitry, and bypass capacitors. Low ohmic contact resistance and good control of MIM capacitance values have been demonstrated which were achieved by careful monitoring of the associated fabrication processes. Yield limiting factors affecting MIM capacitors and FET's have been discussed and some preliminary data on overall circuit yields have been presented. High dc yield of typical amplifier circuits has been shown indicating that the above described MMIC fabrication process has the potential for achieving high overall yields in a production environment. Based on the data presented, it is expected that GaAs MMIC modules with multicircuit complexity can be fabricated with acceptable yield.

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Aditya Gupta received the B. Tech. degree in 1973 from the Indian Institute of Technology, Kanpur, India, and the M.S. and Ph.D. degrees from Cornell University, Ithaca, NY, in 1975 and 1978, respectively.

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